REMARKS

Claims 1, 16, and 20 have been amended.

Claim 15 has been cancelled.

Claims 2, 7-8, were previously cancelled.

Claims 1, 3-6, 9-14, and 16-25 are pending.

Claim 15 was objected to as improperly depending from a cancelled claim. Claim 15 has been cancelled due to the clarifying amendments made to independent Claim 1.

Claims 1, 3-6, and 9-14, and 16-25 stand rejected under 35 USC 103(a) as being unpatentable over the combination of U.S. Patent No. 6,130,967 issued to *Lee et al* and U.S. Patent No. 6,304,958 issued to *Kiuchi et al.*

The Applicant respectfully traverses, and requests that these rejections be reconsidered and withdrawn, for at least the following exemplary reasons.

Lee et al. disclose an image bus ring (14) that is configured to support communication between one image interface (24), one image disk interface (16) and multiple field of view or image processing modules (28, 30, 32, 34). The image bus ring is a single shared bus having high enough bandwidth to allow data communication between the image processing modules and the image interface and image disk interface. In addition to the image bus ring, *Lee et al.* also teach that the image processing modules are coupled to a system bus (50).

Kiuchi et al. disclose various designs for a microcomputer. *Kiuchi et al.* teach that multiple address and data buses can be used to interface with multiple memories. *Kiuchi et al.* teach that each memory is connected (i.e., hardwired) to specific address and data buses. For example, see *Kiuchi et al.* Fig. 34. *Kiuchi et al.* use this divided and hardwired configuration to allow simultaneous data transfer in parallel (see, e.g., column 43, lines 40-44) for these "completely divided" hardware resources.

Independent **Claim 1** is drawn to an apparatus that includes a plurality of logic modules, a plurality of bus interfaces and a plurality of buses. As recited, at least two logic modules are configured to selectively process image related data according to different image processing algorithms and unlike *Lee et al.* each bus interface is operatively coupled to a corresponding logic module. Further contrary to the teachings of *Lee et al.*, the plurality of buses includes a memory bus, a first support bus and a second support bus. As recited and unlike either *Lee et al.* and/or *Kiuchi et al.*, each bus interface is **selectively programmably configurable** to operatively couple the corresponding logic module to at least a programmably selected one of the first support bus and the second support bus **in response to at least one programming control input** to selectively route at least a portion of the image related data between the at least two logic modules for processing in accordance with **a programmable data processing order**.

Lee et al. or *Kiuchi et al.* (alone or in combination) fail to disclose or reasonably suggest such an apparatus as recited in Claim 1. More specifically, these references do not disclose or suggest:

(1) having multiple support buses, rather they employ a single high bandwidth bus that is always coupled to each of the image processing modules;

(2) having a separate bus interface for each image processing module, or any other capability that allows for the selective operative coupling of individual modules to different support buses in response to a control signal;

(3) having at least two logic modules configured to selectively process image related data according to different image processing algorithms, but rather different fields of view, and wherein the control signal causes selective routing of image related data between logic modules through an operatively coupled support bus in accordance with a data processing order.

(4) bus interfaces that are selectively programmably configurable to operatively couple logic modules to at least a programmably selected one of the first support bus and the second support bus in response to at least one programming control input to selectively route at least a portion of the image related data between the at least two logic modules for processing in accordance with a programmable data processing order.

For at least these reasons and others **Claim 1**, and consequently **Claims 3-6, 9-14** which depend there from, are clearly patentable over the cited art.

Independent **Claim 16** has also been amended and is drawn to an apparatus that includes, a plurality of logic modules wherein each logic module

is configured to selectively process image related data according to a different image processing algorithm, a plurality of bus interfaces wherein each bus interface is operatively coupled to a corresponding logic module, and a plurality of buses, including at least a memory bus, a first support bus and a second support bus, that are operatively coupled to the plurality of bus interfaces. As recited, each of the plurality of bus interfaces is selectively programmably configurable to route image related data through either the first support bus or the second support bus to the corresponding logic module for processing in accordance with a programmable data processing order.

Lee et al. and/or *Kiuchi et al.* fail to disclose or reasonably suggest the apparatus as recited in **Claim 16**, and dependent **Claims 17-19**, for at least the same reasons as stated above with regard to Claim 1. For example, the cited art fails to disclose or suggest bus interfaces that are selectively programmably configurable to route image related data through either the first support bus or the second support bus to the corresponding logic module for processing in accordance with a programmable data processing order.

Independent **Claim 20** has been amended and is drawn to an image processing device that includes a plurality of buses including at least a memory bus, a first support bus and a second support bus, memory suitable for storing image related data, a memory bus interface coupled to the memory bus and the memory and configured to provide access to the memory via the memory bus, a plurality of logic modules, each logic module being configured to process image related data according to a different image processing algorithm, and a plurality of bus interfaces, each bus interface being coupled to a corresponding logic module, the first support bus, the second support bus and the memory bus, and selectively programmably configurable to route the image related data through the first support bus or the second support bus to the

plurality of logic modules for processing in accordance with a data processing order.

Lee et al. and/or *Kiuchi et al.* fail to disclose or reasonably suggest the apparatus as recited in **Claim 20**, and dependent **Claims 21-25**, for at least the same reasons as stated above with regard to Claim 1. For example, the cited art fails to disclose or suggest bus interfaces that are selectively programmably configurable to route the image related data through the first support bus or the second support bus to the plurality of logic modules for processing in accordance with a programmable data processing order.

Conclusion

The pending claims are each clearly patentable over the cited art and as such are in condition for prompt allowance. Applicant respectfully requests reconsideration and withdrawal of the rejections and prompt issuance of the subject application.

Respectfully Submitted,

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